v. *Summary of claimed subject matter*

A. ***Overview***

This inventive claimed subject matter relates to controlling execution of multiple tasks in a processing circuit having multiple processing modules. Temperature problems affecting one of the processing modules can be remedied by considering the effects of heat generated by all of the processing modules, not just the affected processing module.

B. ***Relating Overview to Independent Claims***

Independent claims 1, 5, 8 and 12 are pending in this appeal. Each is set forth below with reference numbers of examples, in parenthesis, and with reference to support in the text and drawings of the Specification and consistent with the Overview provided above.

1. Claim 1

Claim 1 is directed to a method for controlling execution of multiple tasks in a processing circuit (100) which includes several processing modules (12, 14a and 14b).[1] Temperature-associated information is determined at various areas of the processing circuit.[2] If the temperature-associated information indicates that there is an excessive temperature at an area associated with one of the processing modules,[3] parameters for executing tasks on one or more of the adjacent modules are modified in order to reduce the heat generated by the adjacent processing modules, which contributes to the excessive temperature at the first processing module.[4]

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[1] Specification, Figure 10.
[2] Specification, page 15, lines 4-17, page 16, lines 1-7 and 12-23; Figure 10.
[3] Specification, page 15, lines 17-19; Figure 10.
[4] Specification, page 15, lines 19-27 and page 16, lines 12 through page 17, line 9.

This aspect of the invention provides significant advantages over the prior art. If a first processing module exhibits an excessive temperature, the problem can be remedied by adjusting the execution on the tasks of *adjacent* processors. Thus, a critical task on the affected processing module can continue while less critical tasks on adjacent processors are manipulated. Since the operation of multiple processing modules is taken into consideration in response to an excessive temperature at a certain processing module, greater flexibility is affording in addressing temperature problems.[5]

2. Claim 5

Claim 5 is directed to a method for controlling execution of multiple tasks in a processing circuit (100) which includes several processing modules (12, 14a, 14b).[6] A task allocation scenario is generated for allocating multiple tasks among the plurality of processing modules. Prior to executing the tasks, temperature-associated information for various locations in the processing circuit are estimated (step 120)[7] to indicate what would occur if the tasks were in fact executed according to the scenario. From this information, it is determined whether a temperature threshold would be exceeded (step 124).[8]

By creating a scenarios estimate temperature based on multiple tasks being performed on multiple processing modules, a more accurate temperature profile is achieved, and situations that would cause excessive temperatures can be avoided.

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[5] Specification, page 15, lines 14-27.
[6] Specification, Figure 10.
[7] Specification, Figure 11.
[8] Specification, page 16, lines 12-18; Figure 11.

3. Claim 8

Claim 8 is directed to a processing circuit (100) which includes several processing modules for processing multiple tasks (12, 14a, 14b).[9] Temperature-associated information is determined at various areas of the processing circuit.[10] If the temperature-associated information indicates that there is an excessive temperature at an area associated with one of the processing modules,[11] parameters for executing tasks on one or more of the adjacent modules are modified in order to reduce the heat generated by the adjacent processing modules, which contributes to the excessive temperature at the first processing module.[12]

This aspect of the invention provides significant advantages over the prior art. If a first processing module exhibits an excessive temperature, the problem can be remedied by adjusting the execution on the tasks of *adjacent* processors. Thus, a critical task on the affected processing module can continue while less critical tasks on adjacent processors are manipulated. Since the operation of multiple processing modules is taken into consideration in response to an excessive temperature at a certain processing module, greater flexibility is affording in addressing temperature problems.

4. Claim 12

Claim 12 is directed to a processing circuit (100). The processing circuit includes several processing modules for executing multiple tasks (12, 14a, 14b).[13] A task allocation scenario is generated for allocating multiple tasks among the plurality of processing modules. Temperature-associated information for various locations in the

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[9] Figure 10.
[10] Specification, page 15, lines 4-17, page 16, lines 1-7 and 12-23; Figure 10.
[11] Specification, page 15, lines 17-19; Figure 10.
[12] Specification, page 15, lines 19-27 and page 16, lines 12 through page 17, line 9.
[13] Specification, Figure 10.

processing circuit is estimated (step 120)[14] to indicate what would occur if the tasks were in fact executed according to the scenario. From this information, it is determined whether a temperature threshold would be exceeded (step 124).[15]

By creating a scenarios estimate temperature based on multiple tasks being performed on multiple processing modules, a more accurate temperature profile is achieved, and situations that would cause excessive temperatures can be avoided.

5. Claim 15

Claim 15 is directed to a mobile communications device (150) having a plurality of processing modules for executing a plurality of tasks, an antenna for receiving and transmitting signals (160) and receiver/transmitter circuitry (162) coupled to said antenna for sending and receiving audio and data signals.[16] The receiver/transmitter circuitry (162) includes a processing circuit comprising circuitry for determining temperature-associated information is determined at various areas of the processing circuit[17] and circuitry responsive to temperature-associated information indicating an excessive temperature at an area associated with one of the processing modules[18] for modifying parameters for executing tasks on one or more of the adjacent modules are modified in order to reduce the heat generated by the adjacent processing modules, which contribute to the excessive temperature at the first processing module.[19]

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[14] Specification, Figure 11.
[15] Specification, page 16, lines 12-18; Figure 11.
[16] Specification, Figure 13.
[17] Specification, page 15, lines 4-17, page 16, lines 1-7 and 12-23; Figure 10.
[18] Specification, page 15, lines 17-19; Figure 10.
[19] Specification, page 15, lines 19-27 and page 16, lines 12 through page 17, line 9.

vi. Grounds of rejection to be reviewed on appeal

A. Rejections Under 35 U.S.C. §102

Claims 1 through 4 and 8 through 11 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Pat. No. 6,000,036 to Durham.[20] With regard to independent claim 1, the Examiner asserts that Durham discloses a method of controlling an execution of multiple tasks ("operations") in a processing circuit of integrated circuit including several processing modules or functional units, comprising the steps of determining temperature-associated information at various areas of the processing circuit; in response to indicating an excessive temperature at an area associated with a first of the processing modules of first function unit, modifying parameters for executing tasks on one or more adjacent processing modules of second functional units in order to reduce heat generated by the adjacent processing modules and contributing to the excessive temperature at the first processing module.[21]

With regard to dependent claim 2, the Examiner contends that Durham teaches the step of monitoring operations executed by said modules (col. 3, line 55 - col. 4, line 61 of Durham).[22]

With regard to dependent claim 3, the Examiner contends that Durham teaches step of calculating power dissipation information at various locations in said processing circuit (citing col. 4, lines 32-61 of Durham).[23]

With regard to dependent claim 4, the Examiner contends that Durham teaches the step of calculating a current temperature at various locations in said processing circuit (citing col. 3, line 55 - col. 4, line 61 of Durham).[24]

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[20] Office Action of December 15, 2005 by reference to the Office Action of June 16, 2005.
[21] Office Action of June 16, 2005, page 2.
[22] Office Action of June 16, 2005, page 2.
[23] Office Action of June 16, 2005, pages 2-3.

Claims 8 through 11 are rejected for the same reasons as Claim 1 through 4.[25]

B. ***Rejections Under 35 U.S.C. § 103***

Claims 5-7 and 12-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,828,568 to Sunakawa in view of U.S. Pat. No. 6,000,036 to Durham.[26] With regard to claim 5, the Examiner contends that Sunakawa discloses a method for controlling an execution of multiple tasks in a processing circuit including a plurality of processing modules, wherein (1) a task allocation scenario (e.g. priority scheduling) for allocating multiple tasks among the plurality of processing modules is generated, (2) prior to executing the tasks, temperature-associated information (e.g. power) in the processing circuit is estimated as would occur if the tasks were executed according to the scenario (citing, col. 2, lines 16-26; col. 9, line 25 – col. 10, line 35 of Sunakawa), and (3) whether a power threshold would be exceeded by executing the tasks according to the scenario is determined (citing col. 8, lines 42-54; col. 10, line 36 – col. 12, line 24 of Sunakawa).[27]

The Examiner states that Sunakawa does not show the step of estimating temperature-associated information for various locations in the processing circuit and determining whether a temperature threshold would be exceeded, but instead relies on Durham for this teaching.[28] The Examiner contends that Durham discloses a method for controlling an execution of multiple tasks (e.g. operations) in a processing circuit, as shown in Figure 1 of Durham, using a plurality of processing modules or functional units (citing the Abstract and Fig. 1; col. 3, lines 17-54 of Durham. The Examiner further contends that Durham teaches the step of: (1) allocating multiple tasks among the

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[24] Office Action of June 16, 2005, page 3.
[25] Office Action of June 16, 2005, pages 3-4.
[26] Office Action of December 5, 2005.
[27] Office Action of December 5, 2005, page 2.
[28] Office Action of December 5, 2005, page 3.

plurality of processing modules (citing col. 1, line 60 — col. 2, line 6 of Durham), (2) prior to executing the tasks (citing col. 4, lines 20-31 of Durham), estimating temperature-associated information for various locations in the processing circuit (citing col. 3, line 55 - col. 4, line 31 of Durham) and determining whether a temperature threshold would be exceeded by executing the tasks (citing col. 4, lines 31-61 of Durham).[29]

The Examiner contends that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Sunakawa to include estimating temperature-associated information for various locations in the processing circuit and determining whether a temperature threshold would be exceeded by executing the tasks according to the scenario as taught by Durham.[30]

With regard to dependent claim 6, the Examiner contends that the step of generating a task allocation scenario in Sunakawa inherently comprises the step of receiving a task list describing the tasks to be executed and a task model describing the tasks (citing col. 9, line 54 — col. 10, line 2 of Sunakawa).[31]

With regard to dependent claim 7, the Examiner contends that the task model in Sunakawa inherently includes initial area-specific power dissipation estimates for each task (citing col. 9, line 54 — col. 10, line 2; col. 13, lines 39-47 of Sunakawa), wherein it is possible to calculate the power dissipation from measured and probabilistic power consumption (as noted in the Specification of the instant application 09/932361 on page 11, lines 16-21).[32]

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[29] Office Action of December 5, 2005, page 3.
[30] Office Action of December 5, 2005, page 3.
[31] Office Action of December 5, 2005, pages 3-4.
[32] Office Action of December 5, 2005, page 4.

Claims 12 through 14 are rejected on the same basis as claims 5 through 7.[33]

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,718,164 to Korneluk et al in view of Durham.[34] Regarding claim 15, the Examiner contends that Korneluk discloses a mobile communications device (citing the Abstract and Fig. 7) comprising: (1) a plurality of processing modules for executing a plurality of tasks (citing col. 9, lines 43-48, and col. 10, lines 23-27 of Korneluk); (2) an antenna for receiving and transmitting signals; and (3) receiver/transmitter circuitry coupled to said antenna for sending and receiving audio and data signals (citing col. 9, line 66 - col. 10, line 13 of Korneluk), with the receiver/transmitter circuitry including a processing circuit comprising: (a) circuitry for determining temperature-associated information at various areas of the processing circuit (citing col. 10, lines 13-30 of Korneluk) and (b) circuitry for executing tasks or data communication on a plurality of processing modules responsive to said temperature-associated information to prevent problems associated with one or more areas exceeding a temperature threshold (citing col. 9, lines 16-36 and col. 10, line 44 -. col. 11, line 65 of Korneluk).[35]

The Examiner states that Korneluk does not teach circuitry for modifying parameters for executing tasks on one or more adjacent processing modules, but claims that this element is provided by Durham, for reasons stated above in connection with the §102 rejection of claim 1.

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[33] Office Action of December 5, 2005, page 4.
[34] Office Action of December 15, 2005 by reference to the Office Action of June 16, 2005.
[35] Office Action of June 16, 2005, pages 5-6.

C. ***Double Patenting Rejections***

Claims 1 through 15 are provisionally rejected on the ground of nonstatutory double patenting over claims 1, 4-7, 10-12, 14-20, and 22-26 of copending U.S. Application No. 09/932,136.[36]

The Examiner notes that a nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s).[37] The Examiner contends that the disclosure and the pending claims of the referenced copending application and the instant application are claiming common subject matter, as follows: controlling executing of multiple tasks in a processing circuit including several processing modules.

[36] Office Action of December 5, 2006, page 4.
[37] Office Action of December 5, 2005, page 4.

vii. Argument

It is axiomatic, in the patent law, that a *prima facie* obviousness determination of patent claims requires teachings from the prior art itself to appear to have suggested the claimed subject matter to a person of ordinary skill in the art.[38] If the Examiner fails to establish a *prima facie* case, the rejection is improper and should be overturned on appeal.[39] Appellants respectfully submit that the final rejection fails to meet this standard. Instead, the teachings of the applied prior art, properly interpreted, fall short of the requirements of each of the claims, and there is no suggestion from the prior art to modify those teachings in such a manner as to reach the claims on appeal in this case.

A. Rejections Under 35 U.S.C. § 102

1. Claims 1-4, 8-11 and 15

Durham addresses a problem that is similar to that described in the present application, but the solution proposed by Durham is significantly different that the current invention. The problem concerns the formation of localized hot spots which can cause failures in a processing circuit. The Durham device prevents hot spots by steering instructions to one of a plurality of substantially equivalent functional units. Power dissipation is measured in each area where a functional unit is located. If the power dissipation within an area exceeds a predetermined amount, a localized heating problem exists within the area. To remedy the localized heating problem in Durham, an instruction intended for the affected processor is dispatched or routed to one of the other functional units located in an area that is not experiencing a localized heating problem.[40]

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[38] *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).
[39] *Id.*
[40] Abstract, col. 3, line 55 through col. 4, line 61, Figure 4, col. 6, line 24 – 65.

Thus, the Durham reference teaches a scheme of reducing localized hot spots in a processor by diverting instructions away from functional unit experiencing a hot spot to a functional unit not experiencing a hot spot. This approach has a significant drawback – the functional units to which an instruction may be diverted must perform substantially the same function or operation in response to an instruction, although they do not need to be structurally identical.[41] Accordingly, redundant circuitry must be provided to accomplish this method.

It should be noted that in Durham, diverting instructions intended for a particular functional unit to other functional units will decrease the heat generated by the affected functional unit (due to a decrease in activity), but will *increase* the temperature of the other functional units by increasing their activity. Any temperature decrease at the particular functional unit is attributable to a reduction in the number of instructions performed at the particular unit.

Claim 1 is directed to an entirely different method of reducing hot spots. Rather than reducing instructions to a first processing module experiencing the excessive temperature, the present invention modifies parameters for executing tasks on one or more *adjacent* processing modules in order to reduce heat generated *by the adjacent processing modules* and contributing to the excessive temperature at the first processing module. By reducing heat generated by the *adjacent* processing modules (which are not necessarily operating at an excessive temperature), the temperature at the first processing module will be reduced.

The method presented by claim 1 is substantially different than that proposed by Durham. Durham does not modify parameters for executing tasks on one or more adjacent processing modules *in order to reduce heat generated by the adjacent processing*

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[41] Durham, col. 3, lines 45-54.

modules; if anything, Durham increases the heat generated by the adjacent processing modules.

The Examiner states that Durham clearly discloses this limitation in col. 4, lines 32-61. The passage cited by the Examiner is repeated below:

> For example, suppose measured or estimated power dissipation within the first area 102 exceeds a predetermined amount. A localized heating problem is, therefore, detected within the first area 102 and this information is relayed to the power down control unit 116 via signal line 118. As such, the power estimator 110 has informed the dispatch unit 114 that a localized heating problem is occurring in the first area 102. Suppose further that the next pending instruction was scheduled for the first functional unit 106 within first area 102, and that another area 104 has a corresponding duplicate ("duplicate" meaning that another functional unit either is identical in form or function for at least that specific operation associated with the instruction) functional unit 108. The dispatch unit 114 then sends the instruction to the second functional unit 108 to perform the required operation and enables the second functional unit 108 via a signal line 124. In addition, the dispatch unit 114 disables the first functional unit 106 via a signal line 120 thereby placing the first functional unit 106 into a low power mode. This reduces the power dissipation within the first area 102 and further reduces both the localized heating problem within the first area 102 and the possibility of catastrophic failure due to overheating. When the localized heating problem in the first area 102 is no longer a problem and/or the first functional unit 106 is required for operation, the dispatch unit 114 enables the first functional unit 106 to receive the next instructions. As will be appreciated, some applications may force the functional unit 106 to operate, thereby neglecting the detected localized heating problem in its area, in order to attain a certain system throughput or other advantages.

The passage cited by the Examiner specifically states that instructions intended for the first functional unit are diverted to a second functional unit and that the first functional unit is placed in a low power mode. The present invention, as defined by claim 1, works in a much different fashion. In a practical situation, various processors

will have various designs which allow them to perform certain functions at high efficiency. For example, a particular processing module in a device might be designed to generate video from an incoming signal. Rather than degrade the performance of this processing module in response to a detected hot spot, the present invention seeks to reduce heat from adjacent processing modules to allow the particular processing module to continue processing video information at full speed.

Because of the significant and important difference between the subject matter of independent claims 1, 8 and 15 and the teaching of Durham, Appellants submit that independent claim 1 and dependent claims 2-4 are novel over Durham. For the reasons stated above, Appellants also submit that claims 8-11 are novel over Durham.

In claim 15, Korneluk is added merely to show a mobile communication device; it does not show any other element of the claim; specifically, it does not show circuitry for modifying parameters for executing tasks on one or more *adjacent* processing modules in order to reduce heat generated *by the adjacent processing modules* and contributing to the excessive temperature at the first processing module.

Accordingly, Appellants submit that claim 15 is novel and unobvious over the combination of Durham and Korneluk.

B. Rejections Under 35 U.S.C. § 103

1. Claims 5-7 and 12-14

The Sunakawa reference shows a system where multiple tasks are executed by a *single* processor. Some of the tasks may use a device external to the processor, such as an I/O device, during their operation. Instead of multitasking using equal, alternating time periods,[42] a task which uses one or more devices (external to the processor) with

[42] See Sunakawa, Figure 5A, where tasks A, B and C are executed using interleaved execution periods.

the largest power consumption is given higher priority in order to complete the task in a shorter period of time. By completing the high priority task in a shorter time period, power to the device (or devices) can be turned off earlier, thereby reducing the power consumed by the device.[43] In a second embodiment (cited by the Examiner in the Office Action) initiating a device pursuant to a task is delayed if turning on the device would exceed power limits.[44] In a third embodiment, increased power due to a device's transition from a high-power mode to a low-power mode is taken into consideration deciding upon whether to place the device in a low power mode once a task's access to a device is complete.[45] In a fourth embodiment, the hysteresis of intervals between accesses to the device is recorded (and averaged). This information is used in the determination of whether a device should transition to a low-power mode after the end of an access.[46] In a fifth embodiment, the transition of a hard disk drive is made with consideration of whether virtual memory is on or off.[47] In a sixth embodiment, a transition to a low power mode is made in consideration of a delay time associated with returning to a high power mode.[48]

The primary goal of Sunakawa is maximizing the time period in which devices external to the processor can be placed in a low power mode (or, in an alternative phrasing of the statement, minimizing the time that devices external to the processor are in a high-power mode). This is accomplished in Sunakawa by accelerating the completion of a task which uses the devices with the most power by delaying the execution of other tasks. This is shown in particular detail in Figures 5A and 5B. In Figure 5A, where tasks A, B and C are executed using equal, alternating processing cycles, I/O unit C is powered from time "0" to "t2" (t2 is equal to t1 - the time necessary

[43] Sunakawa, Abstract and column 8, line 42 through column 9, line 5.
[44] Sunakawa, column 11, line 38 through column 12, line 9.
[45] Sunakawa, column 13, line 48 through column 14, line 34.
[46] Sunakawa, column 17, line 60 through column 18, line 16.
[47] Sunakawa, column 18, lines 17 – 37.

to complete task C using equal alternating execution cycles – plus t_{idle} – the time for I/O unit C to power down after the start of a period of inactivity). In Figure 5B, task C is given two execution cycles for every execution cycle given to task A or task B; hence, task C completes at t3 (where t3 < t1). Accordingly, I/O unit C can power down by t4 (where t4 < t2). The second embodiment of Sunakawa, as cited by the Examiner, when a task makes an access to a device which is currently in a power-saving mode, the current consumption power of the circuit is detected to determine whether the device can be started. If so, a timer determines the point at which the device is stabilized. If the device can not be started due to power considerations, the task which made a request to access the device is changed to a waiting state. When other devices are turned off, freeing up power, the requested device is turned on.

The Examiner concedes that Sunakawa does not show the step of estimating temperature-associated information for various locations in the processing circuit and determining whether a temperature threshold would be exceeded, but instead relies on Durham for this teaching.[49] Durham shows none of the steps of claim 5. Durham does not show generation of a task allocation scenario for allocating multiple tasks among a plurality of processing modules. The portion of Durham cited by the Examiner (col. 1, line 60 through col. 2, line 6) is merely is a collection of general statement of the instruction steering described above. Durham does not generate task scenarios – it diverts the next instruction away from a functional unit with a temperature problem to a functional unit without a temperature problem.

Durham also does not show estimating temperature-associated information for various locations in the processing circuit *as would occur if the tasks were executed according to the scenario*. Durham has no scenarios upon which to estimate temperature-

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[48] Sunakawa, column 18, lines 38-65.
[49] Office Action of December 5, 2005, page 3.

associated information. The power estimators 110, 112 measure or estimate power dissipation within their associated areas (col. 3, lines 55-59). From the measured or estimated power within the areas, the power estimators determine whether the power in the area exceeds a given level. If the power exceeds the level, then a heating problem exists (col. 3, lines 59-66). Thus, Durham estimates current temperature based on *current actual* power dissipation. This varies significantly from the present invention where temperature information is estimated based on a *scenario* upon which temperature information is *estimated*.

Durham also does not determine whether a temperature threshold would be exceeded by executing the tasks according to the scenario. Again, Durham only looks at the current state of the device, i.e., whether the current power exceeds a threshold in a given area, not whether a proposed scenario would result in excessive temperature if the tasks were executed according to the scenario.

Additionally, Sunakawa does not show the other steps of claim 5. Sunakawa does not show the step of generating a task scenario for allocating multiple tasks among a plurality of processors. Instead, Sunakawa shows the step of changing priorities associated with a plurality of tasks to be executed on a *single* processor. Further, Sunakawa does not determine whether a temperature threshold would be exceeded by executing the tasks according to a scenario. Sunakawa only makes a decision not to turn on a device if power thresholds would be exceeded *at the time that the device is to be enabled*. This is a much different solution than the present invention where scenarios are generated *prior to executing the tasks*.

Accordingly, Appellants submit the independent claim 5 and dependant claims 6-7 are novel and unobvious over the teachings of Sunakawa and Durham.

For reasons stated above in connection with claims 5-7, Appellants submit that claims 12-14 are novel and unobvious over the teachings of Sunakawa and Durham as well.

C. ***Rejections Under Non-Statutory Double Patenting***

The most recent version of the claims (and the version of the claims at the time of the rejections) of the '136 application is given below:

> 1. A method of generating energy profiles for a specific task in a processing device executing multiple tasks, comprising the steps of:
>
> receiving a first task identifier indicative of an active task in a processing component;
>
> receiving hardware activity signals each indicative of a hardware event in the processing device;
>
> storing a second task identifier indicating a task to be monitored;
>
> comparing the first and second task identifiers and generating a predetermined signal if the first and second task identifiers match;
>
> measuring activity corresponding to the task to be monitored by counting hardware activity signals received during generation of said predetermined signal.
>
> 4. The method of claim 1 further comprising:
>
> periodically updating with a period T an energy profile responsive to said measuring step during operation of said processing device.
>
> 5. The method of claim 4 and further comprising the step of executing a plurality of tasks in accordance with a scenario defining scheduling of said plurality of tasks and modifying said scenario responsive to said step of updating an energy profile.
>
> 6. The method of claim 1 and further comprising the step of performing a debugging operation responsive to said measuring step.

7. A processing device for multitasking multiple tasks comprising:

circuitry for receiving a first task identifier selected from among a plurality of possible task identifiers indicative of an active task in a processing component;

circuitry for receiving hardware activity signals each indicative of a hardware event in the processing device;

a memory for storing a plurality of second task identifier, each second task identifier corresponding to a task to be monitored;

a comparator for comparing the first and second task identifiers and generating a predetermined second task identifier match signal if the first task identifier matches a corresponding one of said second task identifiers;

a plurality of counters, each counter corresponding to one of said stored plurality of second task identifiers, each counter enabled to count said hardware activity signals when said comparator generates a corresponding predetermined second task identifier match signal.

10. The processing device of claim 7 wherein:

said processing device is operable to periodically update with a period T an energy profile from counts of said plurality of counters during operation of said processing device.

11. The processing device of claim 10 wherein said plurality of tasks are executed in accordance with a scenario defining scheduling of said plurality of tasks and said scenario is updated responsive to said step of updating an energy profile.

12. The processing device of claim 7 and further comprising circuitry for implementing a debugging operation responsive to values in said plurality of counters.

14. The method of claim 1 wherein:

said hardware event in the processing device includes a cache miss.

15. The method of claim 1 wherein:

said hardware event in the processing device includes a translation lookaside buffer miss.

16. The method of claim 1 wherein:

said hardware event in the processing device includes a non-cacheable memory access.

17. The method of claim 1 wherein:

said hardware event in the processing device includes a wait time.

18. The method of claim 1 wherein:

said hardware event in the processing device includes a read/write requests for a predetermined resource.

19. The method of claim 4 wherein:

said period T corresponds to a thermal time constant of the processing device.

20. The processing device of claim 7 wherein:

said hardware event in the processing device includes a cache miss.

22. The processing device of claim 7 wherein:

said hardware event in the processing device includes a translation lookaside buffer miss.

23. The processing device of claim 7 wherein:

said hardware event in the processing device includes a non-cacheable memory access.

24. The processing device of claim 7 wherein:

said hardware event in the processing device includes a wait time.

25. The processing device of claim 7 wherein:

said hardware event in the processing device includes a read/write requests for a predetermined resource.

26. The processing device of claim 10 wherein:

said period T corresponds to a thermal time constant of the processing device.

The Examiner's only contention with regard to double patenting is that the '136 claims cover common subject matter, namely "controlling executing of multiple tasks in a processing circuit including several processing modules." On other words, the Examiner is basing the double patenting rejection based solely on the claims of the '136 application showing the *preamble* of the present claims.

First, it should be noted that the claims of '136 do not even meet this threshold. No claim in the '136 application is directed to controlling executing of multiple tasks in a processing circuit including *several processing modules*. No claim appears to be directed to multiple processing modules.

Second, for a double patenting rejection, the claims of the present application must be anticipated by, or obvious over, the reference claims. The Examiner contends that the two sets of claims are patentably indistinct because the preamble of the current claims is similar to the preamble of the reference claims. The purpose of the judicially created double patenting doctrine is to prevent an applicant from receiving two patents on a single inventive idea. The Examiner's contention would prevent an applicant on receiving two patents on *two different solutions to a single problem*. Surely, there can be more than one invention directed to the problem of "controlling execution of multiple tasks in a processing circuit including several processing modules".

Third, none of the elements of the independent claims appears to be shown in any of the claims of the '136 application. The claims of the '136 application are directed towards monitoring task activity in a multitasking environment. With regard to claims 1, 8 and 15, the claims of the '136 application do not appear to teach either (1) determining temperature-associated information at various areas of the processing circuit or (2) modifying parameters for executing tasks on one or more adjacent processing modules in order to reduce heat generated by the adjacent processing modules and contributing to the excessive temperature at the first processing module. With regard to claims 5 and 12, the '136 claims to not teach the step of (1) generating a task allocation scenario for allocating multiple tasks among the plurality of processing modules, (2) prior to executing the tasks, estimating temperature-associated information for various locations in the processing circuit as would occur if the tasks were executed according to the scenario, or (3) determining whether a temperature threshold would be exceeded by executing the tasks according to the scenario.

viii. Claims appendix

Listing of Claims:

1. A method for controlling execution of multiple tasks in a processing circuit including several processing modules, comprising the steps of:

determining temperature-associated information at various areas of the processing circuit; and

in response to temperature-associated information indicating an excessive temperature at an area associated with a first of said processing modules, modifying parameters for executing tasks on one or more adjacent processing modules in order to reduce heat generated by the adjacent processing modules and contributing to the excessive temperature at the first processing module.

2. The method of claim 1 wherein said determining step comprises the step of monitoring operations executed by said modules.

3. The method of claim 1 wherein said determining step comprises the step of calculating power dissipation information at various locations in said processing circuit.

4. The method of claim 1 wherein said determining step comprises the step of calculating a current temperature at various locations in said processing circuit.

5. A method for controlling execution of multiple tasks in a processing circuit including a plurality of processing modules, comprising the steps of:

generating a task allocation scenario for allocating multiple tasks among the plurality of processing modules;

prior to executing the tasks, estimating temperature-associated information for various locations in the processing circuit as would occur if the tasks were executed according to the scenario;

determining whether a temperature threshold would be exceeded by executing the tasks according to the scenario.

6. The method of claim 5 wherein said step of generating a task allocation scenario comprises the step of receiving a task list describing the tasks to be executed and a task model describing the tasks.

7. The method of claim 6 wherein the task model includes initial area-specific power dissipation estimates for each task.

8. A processing circuit including a plurality of processing modules for executing multiple tasks comprising:

circuitry for determining temperature-associated information at various areas of the processing circuit; and

circuitry responsive to temperature-associated information indicating an

excessive temperature at an area associated with a first of said processing modules for modifying parameters for executing tasks on one or more adjacent processing modules in order to reduce heat generated by the adjacent processing modules and contributing to the excessive temperature at the first processing module.

9. The processing circuit of claim 8 wherein said determining circuitry comprises circuitry for monitoring operations executed by said processing modules.

10. The processing circuit of claim 8 wherein said determining circuitry comprises circuitry for calculating power dissipation information at various locations in said processing circuit.

11. The processing circuit of claim 8 wherein said determining circuitry comprises circuitry for calculating a current temperature at various locations in said processing circuit.

12. A processing circuit comprising:

a plurality of processing modules for executing multiple tasks; and

circuitry for generating a task allocation scenario for allocating the tasks among the processing modules, estimating temperature-associated information for various locations in the processing circuit as would occur if the tasks were executed according to the scenario and determining whether a temperature threshold would be exceeded if the tasks were to be executed according to the scenario.

13. The processing circuit of claim 12 wherein said circuitry for generating a task allocation scenario comprises circuitry for receiving a task list describing the tasks to be executed and a task model describing the tasks.

14. The processing circuit of claim 13 wherein the task model includes initial area-specific power dissipation estimates for each task.

15. A mobile communications device comprising:

a plurality of processing modules for executing a plurality of tasks;

an antenna for receiving and transmitting signals; and

receiver/transmitter circuitry coupled to said antenna for sending and receiving audio and data signals, said receiver/transmitter circuitry including a processing circuit comprising:

circuitry for determining temperature-associated information at various areas of the processing circuit; and

circuitry responsive to temperature-associated information indicating an excessive temperature at an area associated with a first of said processing modules for modifying parameters for executing tasks on one or more adjacent processing modules in order to reduce heat generated by the adjacent processing modules and contributing to the excessive temperature at the first processing module.

ix. Evidence appendix

None.

x. Related proceedings appendix

None.

xi. Conclusion

For the foregoing reasons, Appellants respectfully submit that the final rejection of claims 1 through 15 is in error. Reversal of the rejection is respectfully requested.

Respectfully submitted,

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